

1. Define PROM? (2 Marks)

Answer:- (Page 356)

The PROM stands for Programmable Read only Memory. It is also nonvolatile and may be written into only once. For PROM, the writing process is performed electrically in the field. PROMs provide flexibility and convenience.

2. How we refer the register to the RTL? Give an example? (2 Marks)

Answer:- (Page 66)

Specifying Registers

The format used to specify registers is

Register Name<register bits>

For example, IR<31..0> means bits numbered 31 to 0 of a 32-bit register named "IR" (Instruction Register).

3. What is the use of modem? (2 Marks)

Answer:- (Page 391)

To interconnect different computers by using twisted pair copper wire, an interface is used which is called modem. Modem stands for modulation/demodulation. Modems are very useful to utilize the telephone network (i.e. 4 KHz bandwidth) for data and voice transmission.

4. What is the advantage of RAID level 0? (2 Marks)

Answer:- (Page 330)

- The user and system data are distributed across all the disks in the array.
- Notable advantage over the use of a single large disk.

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6. Encode the register into binary? R0 TO R7 (3 Marks)

Answer:- (Page 51)

Encoding of the General Purpose Registers.

R0	00000
R1	00001
R2	00010
R3	00011
R4	00100
R5	00101
R6	00110
R7	00111

7. What is the difference multimode fiber and mono fiber which are used as a physical medium of the network? (3 Marks)

Answer:- (Page 391)

Multimode fiber

This fiber has large diameter. When light is injected, it disperses, so the effective data rate decreases. Multimode fiber is used as a physical medium of the network

Mono mode Fiber

Its diameter is very small. So dispersion is small and data rate is very high.

8. What is meant by cycle stealing in the DMA? (3 Marks)

Answer:- (Page 320)

The DMA module takes control of the bus to transfer data to and from memory by forcing the CPU to temporarily suspend its operation. This approach is called Cycle Stealing because in this approach DMA steals a bus cycle.

10. Write the radix conversion algorithm to convert 392_{10} to the base 16? (5 Marks)

Answer:- (Page 335)

According to the above algorithm

$$390/16 = 24(\text{rem}=6), x_0=6$$

$$24/16 = 1(\text{rem}=8), x_1=8, x_2=1$$

$$\text{Thus } 390_{10}$$

$$= 186_{16}$$

11. What is the difference between internal segmentation and external segmentation relevant to the computer storage? (5 Marks)

Answer:-

In fixed partitioning the pages are of fixed size and some space is wasted in the last page. For example if we have page size equal to 2 K and the program size is of 9 K than we have to use 5 pages each of size 2 k. In this case 4 pages fully consumed but the last page has 1 k free memory and it can not be utilized, so this type of fragmentation is called internal fragmentation. It is basically the wastage of space of within the partition.

In variable partitioning the page size is not fixed. In this type of partitioning the page size is variable. So pages are allocated accordingly. If say program A is of size 5 k then 5 k page size is reserved and say another program B comes in having size 3 k so now page size of 3 k is reserved. Now if A program exits and the new program C having size 4 k comes in, it will replace the 5 k partition of program A but the space of 1 K is wasted between program C and program B. This wastage of space is called external fragmentation. It is basically the wastage of space between the partitions.

12. Write the SRC assembly program for the following expression? (5 Marks)

Z = 16(a+b) - 32(c-58)

Answer:- (According to Page 57)

```
ld R1, c ; c is a label used for a memory location
subi R3, R1, 58 ; R3 contains (c-58)
shl R7, R3, 5 ; R7 contains 32(c-58)
ld R4, a
ld R5, b
add R6, R4, R5 ; R6 contains (a+b)
shl R8, R6, 4 ; R8 contains 16(a+b)
sub R9, R7, R8 ; the result is in R9
st R9, z ; store the result in memory location z
```

Q1-Write two lines on connection oriented communication? 2

Answer:- (Page 394)

In this method, same path is always taken for the transfer of messages.

It reserves the bandwidth until the transfer is complete. So no other server could use that path until it becomes free.

Q2-What is the advantage of direct cache memory? 2

Answer:- (Page 361)

Advantage is Simplicity.

برى صحبت سے تنہائی بہتر ہے اور تنہائی سے نیک صحبت بہتر ہے

Q3-Write the drawbacks of DMA? 2

Answer:- (Page 315)

The disadvantage however, would be that an additional DMA controller would be required, that could make the system a bit more complex and expensive. Generally, the DMA requests have priority over all other bus activities including interrupts. No interrupts may be recognized during a DMA cycle.

Q4-What is the difference between selection channel and multiple channels? 3

Answer:- (Page 320)

Selector Channel

It is the DMA controller that can do block transfers for several devices but only one at a time.

Multiplexer Channel

It is the DMA controller that can do block transfers for several devices at once.

Q5-What is the advantage of linker in assembly language program? 3

Answer:- (Page 26)

When developing large programs, different people working at the same time can develop separate modules of functionality. These modules can then be 'linked' to form a single module that can be loaded and executed. The modularity of programs, that the linking step in assembly language makes possible, provides the same convenience as it does in higher-level languages; namely abstraction and separation of concerns. Once the functionality of a module has been verified for correctness, it can be re-used in any number of other modules. The programmer can focus on other parts of the program. This is the so-called "modular" approach, or the "top-down" approach.

What do you know about PROM? Explain.(2 marks)

Answer:- Rep

What do you understand by the assembler of the assembly language? (2 marks)

Answer:- (Page 26)

Programs written in assembly language require translation to the machine language, and an assembler performs this translation. This conversion process is termed as the assembly process.

Consider a LAN using bus topology if we replace the bus with a switch, what change occurs in such a configuration. (2 marks)

Answer:- (Page 385)

If we replace the bus with a switch, the speed of the data transfer will be improved to a great extent.

Name the two classes of instruction set architecture. (2 marks)

Answer:- (Page 32)

- Accumulator based machines
- Stack based machines

Find the average rotational latency if the disk rotates 15000rpm. (3 marks)

Answer:- (Page 324)

The average latency to the desired data is halfway round the disk so

$$\text{Average rotational latency} = (1 / (\text{RPM} / 60)) * 0.5 * 1000$$

$$= 30000 / \text{RPM} = 30000 / 15000$$

$$= 2\text{ms}$$

How shift instructions are useful? When do we use them? (3 marks)

Answer:- (Page 18) [click here for detail](#)

Using shift instructions (shifl, asr, etc.) is faster than **mul** and **div**, if the multiplier or divisor is a power of 2. Shift and logical instructions are used to implement logical expressions and bitwise logical operators in high level languages. Shift instructions for arithmetic operations are more efficient than the corresponding arithmetic instruction.

How the exception may be generated? Difference between external and internal exception.

Answer:- (Page 197)

Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.

External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

Conceder the following point number

$$-6 \times 10^{-3}$$

Find out the sign, significant and exponent from the above example. (3 marks)

Answer:- (Page 347)

Sign = -1

Significand= 6

Exponent= -3

Base = 10= fixed for given type of representation

Does DMA affect the relationship between the memory system and the CPU? Explain (5 marks)

Answer:- (Page 321)

DMA and memory system

DMA disturbs the relationship between the memory system and CPU.

Direct memory access and the memory system

Without DMA, all memory accesses are handled by the CPU, using address translation and cache mechanism. When DMA is implemented into an I/O system memory accesses can be made without intervening the CPU for address translation and cache access. The problems created by the DMA in virtual memory and cache systems can be solved using hardware and software techniques.

Suppose the I/O system with a single disk get an average of 200 I/O request/second assume that the average time for a disk to service and I/O request is 4ms. What is the utilization of I/O system? (5marks)

Answer:- (Page 382)

Time for an I/O request = 4ms

=0.004sec

Server utilization = 200×0.004

= 0.8

Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines

a) How many sets are there in the cache?

b) How many bits of address are required to select a set in cache?

Answer:-

(a)

$256 \times 1024 \div 32 = 8192$ lines of data

$8192 / 4 = 2048$ sets in the cache

A 256KB cache with 32 byte lines contains 8192 lines of data. In a 4-way set associative cache, each set contains 4 lines, so there are 2048 sets in the cache.

(b)

$\log_2(2048) = 11$. Hence 11 bits of the address are required to select the set.

1. The following table shows a partial summary of the ISA for the SRC. Write an assembly language program using the SRC assembly language to evaluate the expression: (5 marks)

$$Z = (7 + 16a) - (8b - c)$$

Answer:-

Answer:- (According to Page 57)

```
ld R1, c ; c is a label used for a memory location
ld R2, b
shl R3, R2, 3
sub R4, R3, R1
ld R5, a
shl R5, 4
addi R6, R5, 7
sub R7, R6, R4
st R7, z ; store the result in memory location z
```

Find the bandwidth of a memory system that has a latency of 30ns, a pre charge time of 10ns and transfers 3 bytes of data per access. (5 marks)

Answer:-

Time between two memory reference
= latency + pre charge time
= 30ns + 10ns
= 40ns

Throughput = $1/40\text{ns}$
= 2.5×10^7 operation/sec

Bandwidth = $3 \times 2.5 \times 10^7$
= 7.5×10^7 bytes/sec

2. Explain the Direct Mapping cache strategy. (5 marks)

Answer:- (Page 360)

In this technique, a particular block of data from main memory can be placed in only one location into the cache memory. It relies on principle of locality.

Cache address is composed of two fields:

- Group field
- Word field

Valid bit specifies that the information in the selected block is valid.

3. How many platters are required for a 40GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter? (5 marks)

Answer:- (Page 325)

The capacity of one platter

$$= 1024 \times 2048 \times 4096$$

$$= 8\text{GB}$$

For a 40GB hard disk, we need $40/8$

$$= 5 \text{ such platters.}$$

1. What do you understand by RAID 2? (3 marks)

Answer:- (Page 331)

In RAID 2, error-correcting code is calculated across corresponding bits on each data disk.

2. Give an example for the logic design level, circuit level and mask level abstractions of digital design. (3 marks)

Answer:- (Page 22)

Logic Design Level

The logic design level is also called the gate level. The basic elements at this level are gates and flip-flops. The behavior is less visible, while the hardware structure predominates.

The above level relates to “logic design”.

Circuit Level

The key elements at this level are resistors, transistors, capacitors, diodes etc.

Mask Level

The lowest level is mask level dealing with the silicon structures and their layout that implement the system as an integrated circuit.

The above two levels relate to “circuit design”.

3. Differentiate between Spatial Locality And Temporal Locality. (3 marks)

Answer:- (Page)

Spatial Locality

This would mean that in a part of a program, if we have a particular address being accessed then it is highly probable that the data available at the next address would be highly accessed.

Temporal Correlation

In this case, we say that at a particular time, if we have utilized a particular part of the memory then we might access the adjacent parts very soon.

4. Suppose an I/O system with a single disk gets (on average) 200 I/O requests/second. Assume that average time for a disk to service an I/O request is 4ms. (3 marks)

Answer:- Rep

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What is the utilization of the I/O system? (3 marks)

Answer:- (Page 381)

Server Utilization = Arrival Rate x Time_q

Server utilization is also called traffic intensity and its value must be between 0 and 1.

Server utilization depends upon two parameters:

1. Arrival Rate
2. Average time required to serve each task

So, we can say that it depends on the I/O bandwidth and arrival rate of calls into the system.

1. Which term do we use to describe a “storage systems” resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques? (2 marks)

Answer:- [click here for detail](#)

RAID is the term used to describe a storage systems' resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques.

2. Differentiate between CPU register and Cache Memory. (2 marks)

Answer:- (Page 33)

In general purpose register machines, a number of registers are available within the CPU. These registers do not have dedicated functions, and can be employed for a variety of purposes. CPU registers are faster than cache memory.

Cache memory is random access memory (RAM) that a computer microprocessor can access more quickly than it can access regular RAM.

3. Write one advantage and one disadvantage of cache design. (2 marks)

Answer:- (Page 361)

Advantage:

Simplicity

Disadvantage:

Only a single block from a given group is present in cache at any time. Direct map Cache imposes a considerable amount of rigidity on cache organization.

4. What is the format of a 0-address instruction set? (2 marks)

Answer:- (Page 36)

0-address instruction

- The code size is 1 byte
- Number of bytes accessed from memory is 10
(1 byte for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 10 bytes)

op code

1 byte

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How many drives do you need a minimum to form RAID 0? (2 marks)

0

Only 1

Minimum 2

Maximum 2

Answer:- [click here for detail](#)

Minimum 2

To establish a RAID 0 volume, a minimum of at least 2 hard disk drives are required. Unlike RAID 1, the number of drives used in the array can be an odd or even number.

What function is performed by the reset operation of a processor? What are the two types of reset operations?

Answer:- (Page 194-195)

The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Hard Reset

The SRC should perform a hard reset upon receiving a start (Strt) signal. This initializes the PC and the general registers.

Soft Reset

The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset results in initialization of PC only.

The reset signal in SRC is assumed to be external and asynchronous.

Q2 What do you know about Hard disk.

Answer:- (Page 323)

Peripheral devices connect the outside world with the central processing unit through the I/O modules. One important feature of these peripheral devices is the variable data rate. Peripheral devices are important because of the function they perform.

A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, before the actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header there is a trailer. Every sector has three parts: a header, data section and a trailer.

Q 3 :- Convert $(0.23)_{10}$ to the base 2 address 2Marks

Answer:- (page 336)

$$0.23 \times 2 = 0.46, f_1 = 0$$

$$0.46 \times 2 = 0.92, f_2 = 0$$

$$0.92 \times 2 = 1.84, f_3 = 1$$

$$0.84 \times 2 = 1.68, f_4 = 1$$

$$0.68 \times 2 = 1.36, f_5 = 1, \dots$$

$$\text{Thus } 0.24_{10} = (0.00111)_2$$

Question no 4

What is meant by Packet switching

Answer:- (Page 387)

A block (an appropriate number of bits) of data is called a packet. Transfer of data in the form packets through different paths in a network is called packet switching. Additional bits are usually associated with each packet. These bits contain information about the packet. These additional bits are of two types: header and trailer. As an example, a packet may have the form shown below:

Header	Word to be transferred	Trailer
--------	------------------------	---------

If we use a 1-bit header, we may have the following protocol:

Header = 0, it means it is a request

Header = 1, Reply

By reading these header bits, a machine becomes able to receive data or supply data. To transfer data by using packets through hardware is very difficult. So all the transfer is done by using software. By using more number of bits, in a header, we can send more messages. For example if n bits are used as header then 2^n is the number of messages that can be transmitted over a network by using a single header.

For a 2 bit header: we may have 4 types of messages:

00 = Request

01 = Reply

10 = Acknowledge request

11 = Acknowledge reply

Question no 6

Classification of fiber optics mode multimode and mono mode?

Answer:- Rep

Question no 7

Consider a 64KB direct-mapped cache with a line length of 32 bytes. (5 marks)

a. Determine the number of bits in the address that refer to the byte within a cache line.

b. Determine the number of bits in the address required to select the cache line

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Answer:- (Page 375)

Address breakdown

$n = \log_2$ of number of bytes in line

$m = \log_2$ of number of lines in cache

a. For the given cache, the number of bits in the address to determine the byte within the line = $n = \log_2 32 = 5$

b. There are $64K/32 = 2048$ lines in the given cache. The number of bits required to select the required line = $m = \log_2 2048 = 11$

Hence $n=5$ and $m=11$

Question no 8

If a DRAM has 512 rows and its refresh time is 9ms. What should be the frequency of row refresh operation on the average?

Answer:- (Page 371)

Refresh time = 9ms

Number of rows = 512

Therefore we have to do 512 row refresh operations in a 9 ms interval, in other words one row refresh operation every $(9 \times 10^{-3})/512 = 1.76 \times 10^{-5}$ second

Question

Structural RTL for not instruction not ra ,rb

Answer:- (Page 160)

Step	RTL
T0-T2	Instruction fetch
T3	$C \leftarrow I(R[rb]);$
T4	$R[ra] \leftarrow C;$

Question

why we use matrix in decoder

Answer:- (Page 352)

A typical one level decoder has n inputs and 2^n output, using one level of gates, each with a fan-in of n . Two level decoders are limited in size because of high gate fan-in. In order to reduce the gate fan-in to a value of 8 or 6, tree and matrix decoders are utilized.

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